## Summary

How much of the CPU specification did you complete (given your group size)? Is there anything you didn’t get to do?

I was working alone, I got most of the CPU circuit complete, I got it to pass a few tests but not all.

What cases do your tests cover? What cases might your tests not have covered?

I did not end up having the time to build any tests.

Briefly describe the design of your control unit.

I unfortunately did not get to this part though I did try. I knew we needed to build the control unit which consisted of the decoder and conditional logic. For the decoder, the main decoder’s truth table was given on page 400 of our textbook and that was the part I was trying to get done. I struggled with implementing the logic as I was not sure how to deal with 2 bit inputs and outputs.

## Process

1. Tell us about the specific steps you took to complete the project. How did you start? What was the sequence of specific improvements you made?

Started by looking in the book to see how the CPU should be implemented. Also used the book to determine the exact bits used for instructions for dataprocessing. I organized my components in a friendly fashion because at first I had wires crossing each all over each other.

**~~If working on a team~~**~~: how did you manage subcircuits, circuit files, and test code so that you could work both independently and collaboratively? Give specific examples. If you changed your strategy, talk about that, too.~~

**If working alone**: how did you organize the components of the circuit? Talking about datapath versus control is one starting point, but you need to discuss specific decisions you faced about the organization.

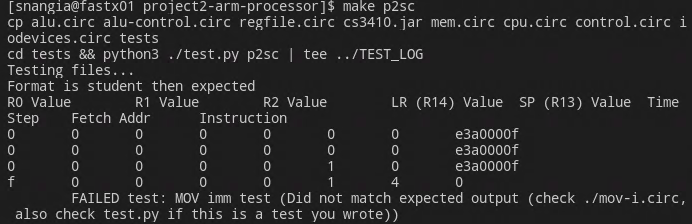
**Since I only worked on CPU**

First I focused on the instruction datapath and used the information from the book to determine all the parts coming from the instruction component. I then focused on the ALU component since the instruction processing was finished, since the ALU needed the ALU control and RegFile. I put those three components near each other so that there was an area specific for those and my organization was better. I then worked on the PC component and placed it away from everything else right below the fetch address output since the PC related to that. I used a fetch address tunnel for PC’s output and also put the output from the PC into an adder to add 4 bits.

## Debugging story

1. Describe a time when your project had an undesired behavior. Give the specific behavior you ***expected*** as well as the specific behavior you ***actually observed***.

My tests continued to fail, and I wasn’t sure why because I figured at least 1 test would have passed after completing the CPU. While the program compiled my student value was not matching the expected value



1. Describe the specific steps you took to investigate the cause of the problem. It should be detailed enough that we can follow your thought process.

I looked into the register file and realized that there was an input for the clock that I did not realize before. I opened the mov-add-reg.circ and right clicked into view main. Through that I was able to double check if all my value were correct for the inputs and outputs. I realised that I had my Rn and Rd values switched thus Rn was going into write register when it should have been going into read register 1. Despite this I was still getting an error and realised that it was due to a missing clock connected to the register.

1. Describe the specific fix you attempted as a result of that investigation. Why did you think this fix would work? What was the new behavior you observed after the fix?

I added the tunnel clock to all of the required circuits it should have been going into. I also ensured the Rm, Rn and Rd tunnels were going into A1, A2 and A3 respectively in the register. I passed 2 tests and my student value matched the expected output.

## ~~(teams of 3+ only) Description of IO~~

~~Describe how we can run and see the output of your IO program. What should we expect to see?~~